TEXAS INSTRUMENTS

TPS71533EVM

LDO Regulator Evaluation Module

User's Guide

May 2003 *Power Management Products Low Power*

SLVU061A

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DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7–24 V and the output current range of 0 mA to 50 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the TPS71533EVM LDO regulator evaluation module. Each EVM PCB contains a SLVP199 test board with a TPS71533DCK low dropout linear regulator as well as supporting passive components. The EVM provides a convenient method of evaluating the performance of the TPS715xx linear regulator family or other SC-70/SOT-323 packaged devices with similar pin-outs.

How to Use This Manual

- Chapter 1—Introduction
- Chapter 2—EVM Test Setup
- Chapter 3—Test Results

Related Documentation From Texas Instruments

- TPS71533 data sheet (literature number SLVS338)

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Chapter 1

Introduction

This user's guide describes the TPS71533EVM LDO regulator evaluation module. Each EVM contains a TPS71533 low dropout linear regulator as well as supporting passive components.

Topic **Page**

1.1 TPS715xx Family of LDO Regulators

The TPS715xx family of LDO regulators is comprised of small SOT–223/PICO packaged regulators capable of delivering 50 mA of output current. Features of the part include:

- 50-mA Low-Dropout Regulator
- 24-V Maximum Input Voltage
- Low 4.25-μA Quiescent Current at 50 mA
- 5-Pin PICO/SC70 (DCK) Package
- Stable With Any Ceramic Capacitor (>0.47 μF)
- Dropout Voltage Typically 100 mV at 50 mA
- Over Current Limitation
- –40°C to 125°C Operating Junction Temperature Range

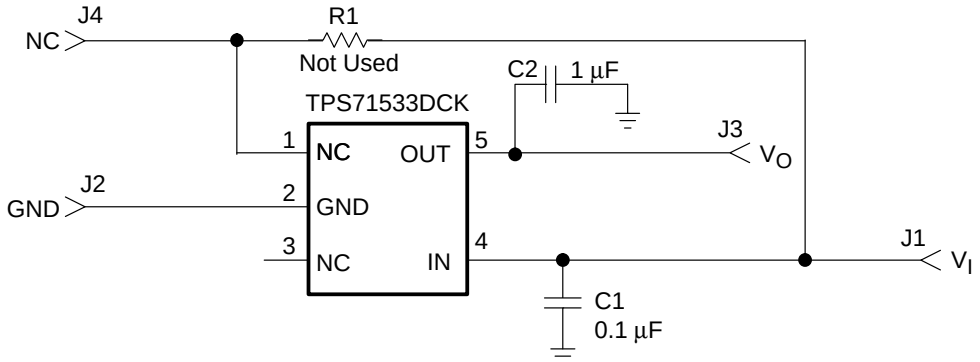
1.2 EVM Design Strategy

The purpose of this EVM is to facilitate evaluation of the TPS715xx family of LDO regulators. Each EVM PCB contains a TPS71533 low dropout linear regulator as well as supporting passive components. Also, the board's small size and side clips facilitate attaching it to other PCBs as a power module.

1.3 Schematic

Figure 1-1 shows the SLVP199 PCB schematic diagram, which is used as the PCB for the TPS71533EVM.

Figure 1–1. Schematic Diagram



1.4 Bill of Materials

Table 1–1 lists materials required for the TPS71533EVM.

Table 1–1. TPS71533EVM Bill of Materials

Qty	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Murata	GRM188R71E104KA01
1	C2	Capacitor, ceramic, 1-μF, 6.3 V, X5R, 10%	603	Murata	GRM188R60J105KA01
4	J1–J4	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA-D36W-0FC
0	R1	Not used	603		
1	U1	IC, regulator, LDO, micropower	SOP-5 (DCK)	TI	TPS71533DCK

1.5 Board Layout

Figures 1–2 through 1-4 show the board layout for the SLVP199 PCB used for the TPS71533EVM.

Figure 1–2. Top Layer

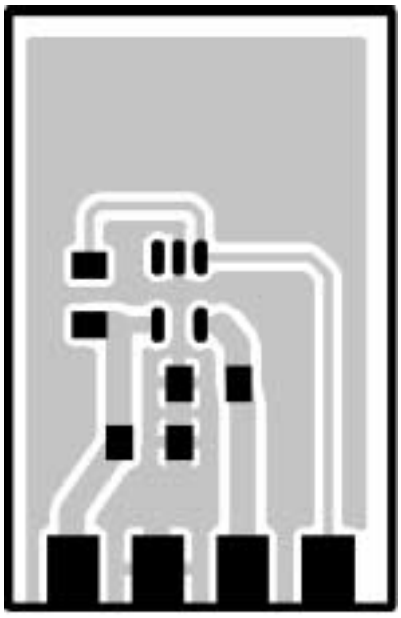


Figure 1–3. Bottom Layer

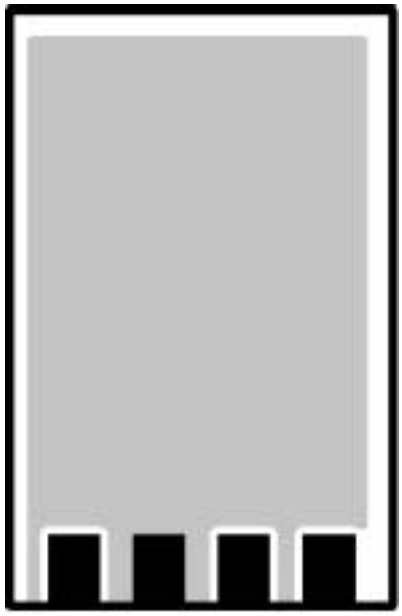
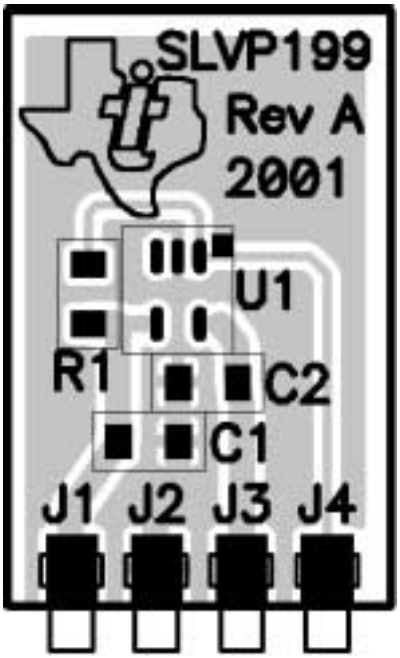


Figure 1–4. Assembly Drawing (top)

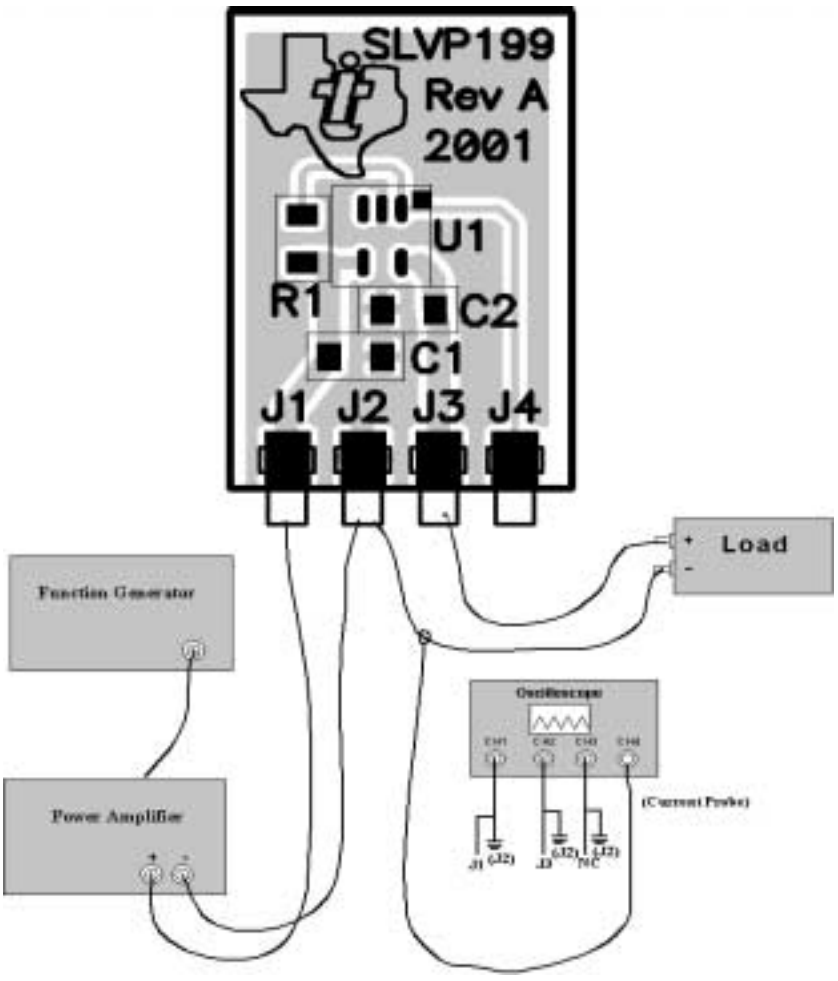


Chapter 2

EVM Test Setup

This chapter provides recommended test equipment and procedures for performing evaluations using the TPS71533EVM. Figure 2–1 shows the test setup.

Figure 2–1. Recommended TPS71533EVM Test Setup



The settings for the test equipment shown in Figure 2–1 are described below:

- Function generator is set to a triangle wave that ramps from 0 V to 8 V, and a period of 10 ms.
- Power amplifier is set to a gain of 3 dB and a minimum slew rate of 5000 V/μs.
- Power supply capable of ±30-V swing and a 0.5-A current limit to power the power amplifier.
- A four-channel oscilloscope with channel one's voltage probe connected to J1 (IN) and channel two's voltage probe connected to J3 (OUT). Using a free channel, connect a current probe around the output load resistance. Set the scope to trigger off of channel one so that one full triangle is displayed on the screen.
- A 66-Ω resistance for 50-mA of output current (or 50-mA electronic load) connected between J3 (OUT) and J2 (GND).

After powering on the amplifier, the input voltage, output voltage, and output current is displayed.

Chapter 3

Test Results

This chapter provides laboratory test results of the TPS71533EVM.

Figure 3–1 shows the input voltage ramp from 0 to just below 24 V (CH1), the 3.3-V regulated output voltage (CH2), and the 50-mA output current (CH4). The scale on CH4 is 20 mA/div.

Figure 3–1. Input Voltage Ramp vs Output Voltage